

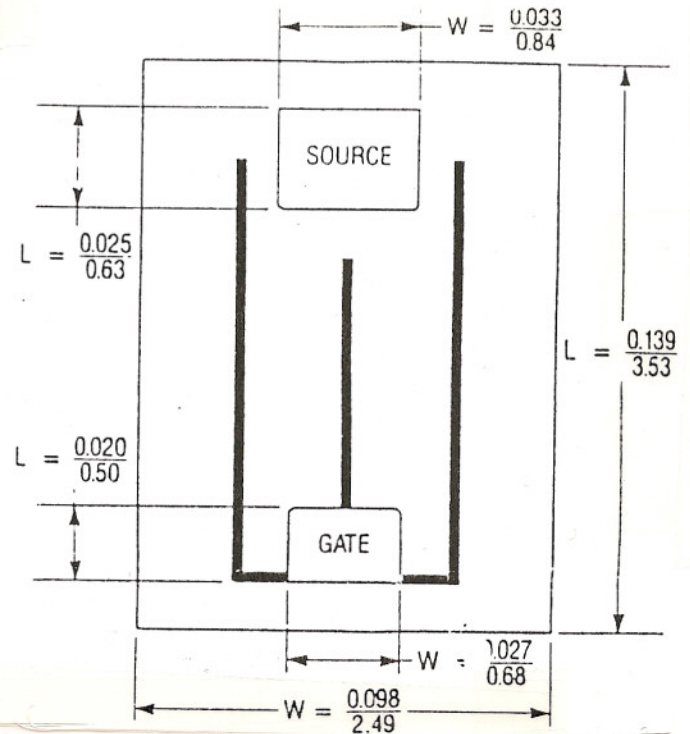


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

HEX-2: 400V, 500V, & 600V, N-CANNEL



The information for this layout is believed to be correct at the time of issue. Please verify your requirements against this information, prior to commencement of any assembly process, as no liability for omission or error can be accepted.

Topside Metal: Al
Backside: Si
Backside Potential:
Mask Ref:
Bond Pads: .004" min

APPROVED BY: CB
MFG: IRI

DIE SIZE: .098" x .139"
THICKNESS: .019"

DATE: 2/8/01
P/N: IRFC420

DG 10.1.2
 Rev A 3-4-99